



PACDN009

Features

- Five channels of ESD protection
- $\pm 8\text{kV}$ contact, $\pm 15\text{kV}$ air ESD protection per channel (IEC 61000-4-2 standard)
- $\pm 15\text{kV}$ of ESD protection per channel (HBM)
- Low loading capacitance (3pF typical)
- Low leakage current is ideal for battery-powered devices
- Available in miniature 8-lead MSOP package
- RoHS compliant (lead-free) finishing

Applications

- Consumer electronic products
- Cellular phones
- PDAs
- Notebook computers
- Desktop PCs
- Digital cameras and camcorders
- VGA (video) port protection for desktop and portable PCs

Product Description

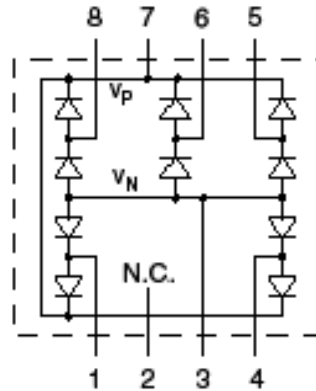
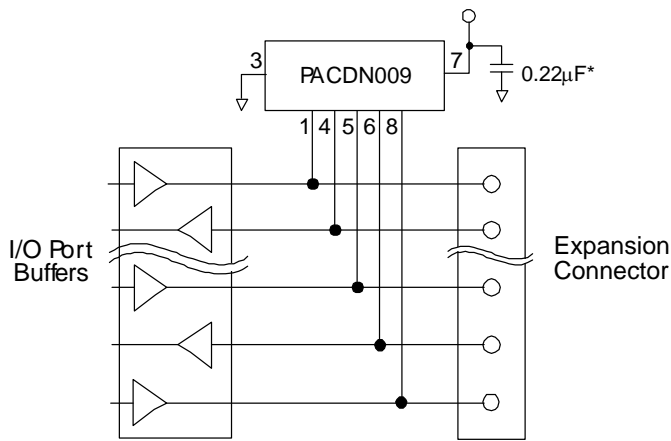
The PACDN009 is a diode array designed to provide 5 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers an ESD current pulse to either the positive (V_p) or negative (V_n) supply. The PACDN009 protects against ESD pulses up to $\pm 15\text{kV}$ Human Body Model (100 pF capacitor discharging through a $1.5\text{K}\Omega$ resistor), and $\pm 8\text{kV}$ contact discharge, per International Standard IEC 61000-4-2.

This device is particularly well-suited for portable electronics (e.g., cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripherals and is ideal for a wide range of consumer electronics products.

The PACDN009 is supplied in an 8-lead MSOP package and is available with RoHS compliant lead-free finishing.

Typical Application Circuit

Electrical Schematic

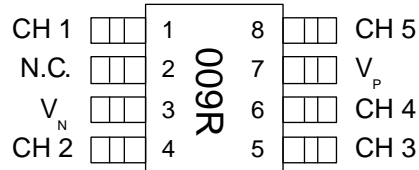


Handheld/PDA ESD Protection

* Capacitor should be placed as close as possible to Pin7

PACKAGE / PINOUT DIAGRAMS

TOP VIEW



PACDN009
8-lead MSOP Package

Note: This drawing is not to scale.

PACDN009

PIN DESCRIPTIONS			
PIN	NAME	TYPE	DESCRIPTION
1	CH 1	I/O	ESD Channel
2	N.C.	-	No connect
3	V_N	GND	Negative voltage supply rail or ground reference rail
4	CH 2	I/O	ESD Channel
5	CH 3	I/O	ESD Channel
6	CH 4	I/O	ESD Channel
7	V_P	Supply	Positive voltage supply rail
8	CH 5	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION			
Leads	Package	Lead-free Finish	
		Ordering Part Number ¹	Part Marking
8	MSOP	PACDN009MR	009R

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage ($V_p - V_n$)	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_n - 0.5)$ to $(V_p + 0.5)$	V
Package Power Rating	200	mW

Note 1: Only one diode conducting at a time.

STANDARD OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage ($V_p - V_n$)	0 to 5.5	V

ELECTRICAL OPERATING CHARACTERISTICS(SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IP	Supply Current	$(V_p - V_n) = 5.5V$			10	μA
VF	Diode Forward Voltage	$I_F = 20mA$	0.65		0.95	V
VESD	ESD Protection	Note 2				
	Peak Discharge Voltage at any channel input, in system	Notes 3	±15			kV
	a) Human Body Model, MIL-STD-883, Method 3015	Note 4	±8			kV
	b) Contact Discharge per IEC 61000-4-2	Note 4	±15			kV
VCL	Channel Clamp Voltage	@ 15kV ESD HBM				
	Positive Transients				$V_p + 13.0$	V
	Negative Transients				$V_n - 13.0$	V
ILEAK	Channel Leakage Current			±0.1	±1.0	μA
CIN	Channel Input Capacitance	@ 1 MHz, $V_p = 5V$, $V_n = 0V$, $V_{IN} = 2.5V$; Note 2 applies		3	5	pF

Note 1: All parameters specified at $T_a = 25^\circ C$ unless otherwise noted. $V_p = 5V$, $V_n = 0V$ unless noted.

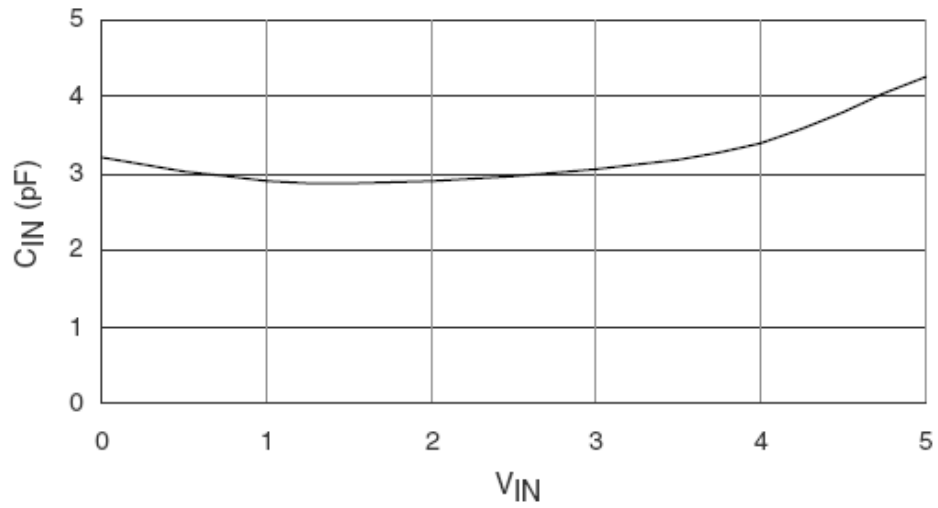
Note 2: From I/O pins to V_p or V_n only. V_p bypassed to V_n with a $0.22\mu F$ ceramic capacitor (see Application Information for more details).

Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge} = 100pF$, $R_{Discharge} = 1.5K\Omega$, $V_p = 5.0V$, V_n grounded.

Note 4: Standard IEC 61000-4-2 with $C_{Discharge} = 150pF$, $R_{Discharge} = 330\Omega$, $V_p = 5.0V$, V_n grounded.

Performance Information

Input Capacitance vs. Input Voltage



Typical Variation of C_{IN} vs. V_{IN}

(V_P = 5V, V_N = 0V, 0.1 μF chip capacitor between V_P and V_N)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to [Figure 1](#), which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2 . The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL} !

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_{CL} equation above, the V_{SUPPLY} term, in reality, is given by $(V_{DC} + I_{ESD} \times R_{OUT})$, where V_{DC} and R_{OUT} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{OUT} of 1 ohm would result in a 10V increment in V_{CL} for a peak I_{ESD} of 10A.

If the inductances and resistance described above are close to zero, the rail-clamp ESD protection diodes will do a good job of protection. However, since this is not possible in practical situations, a bypass capacitor must be used to absorb the very high frequency ESD energy. So for any brand of rail-clamp ESD protection diodes, a bypass capacitor should be connected between the V_P pin of the diodes and the ground plane (V_N pin of the diodes) as shown in the Application Circuit diagram below. A value of 0.22 μ F is adequate for IEC-61000-4-2 level 4 contact discharge protection (± 8 kV). Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Notes AP209, "Design Considerations for ESD Protection" and AP219, "ESD Protection for USB 2.0 Systems"

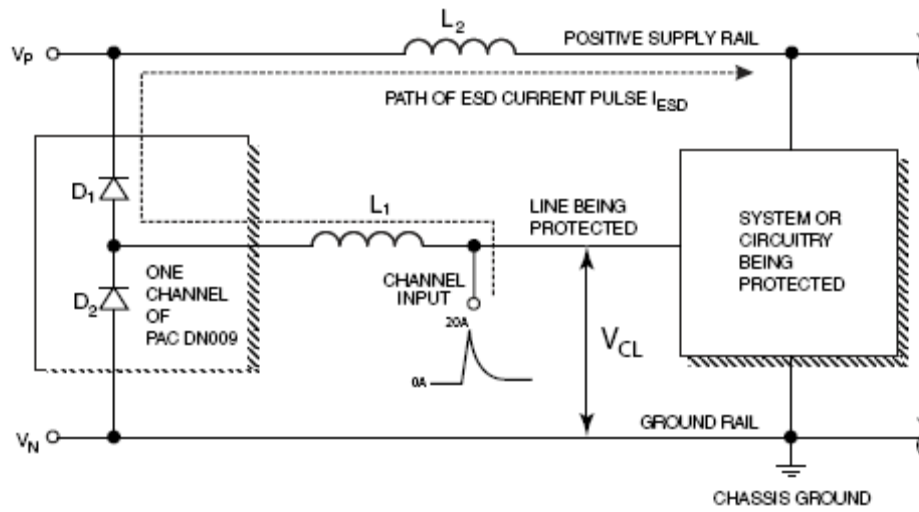


Figure 1. Application of Positive ESD Pulse between Input Channel and Ground

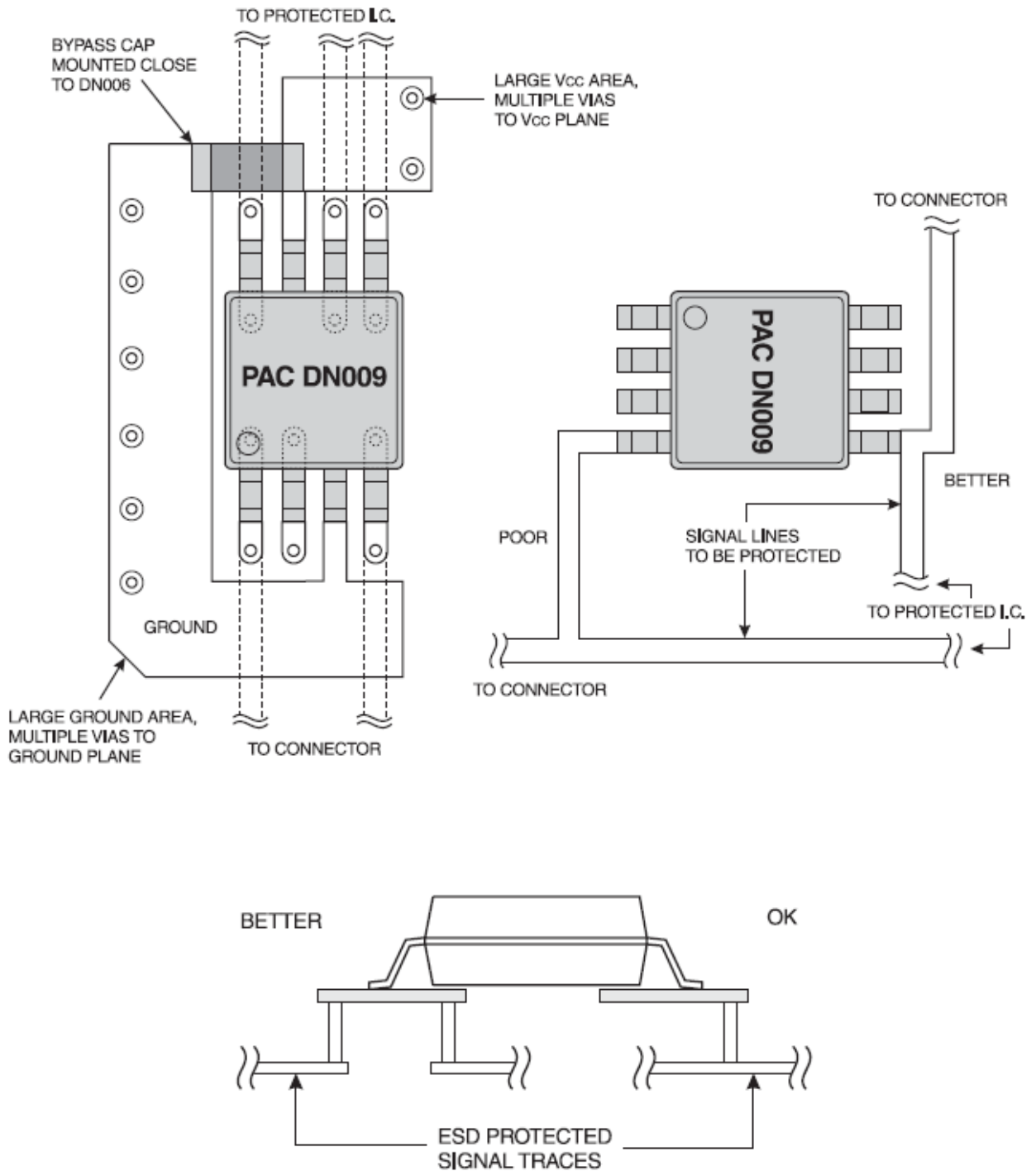


Figure 3. PCB Layout Recommendation

PACDN009

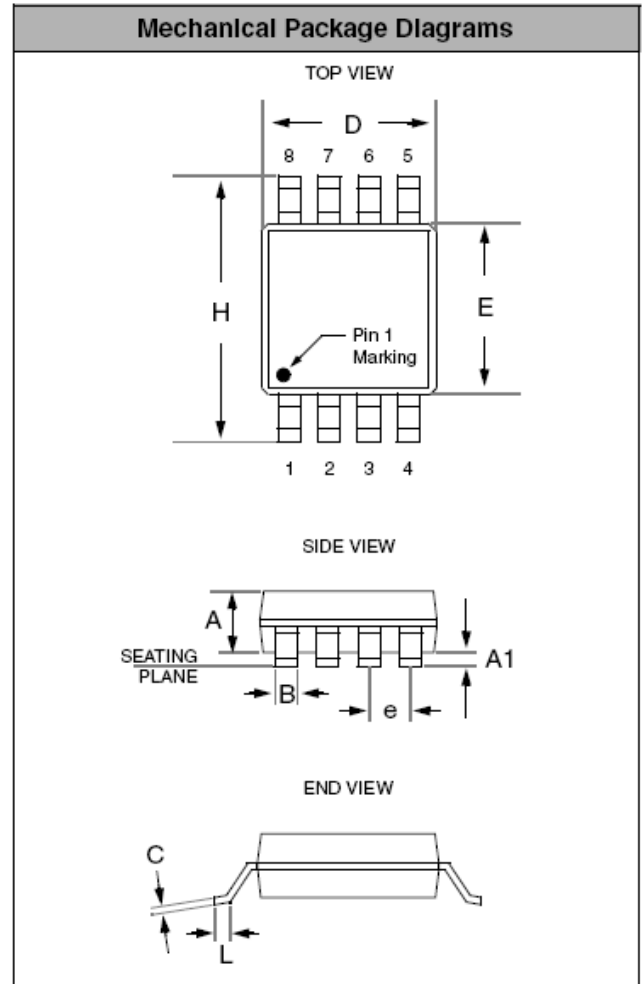
Mechanical Details

MSOP-8 Mechanical Specifications, 8 pin


The PACDN009 is supplied in a 8-pin MSOP package. Dimensions are presented below.

For complete information on the MSOP-8, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.75	0.95	0.030	0.037
A1	0.05	0.15	0.002	0.006
B	0.28	0.38	0.011	0.015
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.016	0.028
# per tape and reel	4000 pieces			
Controlling dimension: millimeters				



Dimensions for MSOP-8 Package

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855
Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative